	Type	L #	Hits	Search Text	DBs
1	BRS	L1	1	"5768567".pn. and transfer	USPAT
2	BRS	L2	1	"5768567".pn. and coherent	USPAT
3	BRS	L3	0	"5768567".pn. and virtual	USPAT
4	BRS	L4	0	"5768567".pn. and (high adj performance)	USPAT
5	BRS	L5	1	"5768567".pn. and high	USPAT
6	BRS	L6	0	"6678645".pn. and version	USPAT
7	BRS	L7	0	"5768567".pn. and version	USPAT
8	BRS	L8	1	"5768567".pn. and state	USPAT
9	BRS	L9	1	"5768567".pn. and state	USPAT
10	BRS	L10	0	"5768567".pn. and (state adj information)	USPAT
11	BRS	L11	0	((co-simulation) same FPGA) and (state adj information)	USPAT
12	BRS	L12	13	((co-simulation) and FPGA) and (state adj information)	USPAT
13	BRS	L13	10	((co-simulation) and FPGA) and (state adj information) and emulation and HDL	USPAT
14	BRS	L14	0	((co-simulation) and FPGA) and (state adj information) and emulation and HDL AND C++	USPAT
15	BRS	L15	0	((co-simulation) and FPGA) and (state adj information) and emulation and HDL and C++	USPAT
16	BRS	L16	10	((co-simulation) and FPGA) and (state adj information) and emulation and HDL and C	USPAT
17	BRS	L17	10	(co-simulation) and FPGA and (state adj information) and emulation and HDL and C	USPAT

	Type	L #	Hits	Search Text	DBs
18	BRS	L18	0	(co-simulation) and FPGA and (state adj information) and emulation and HDL and C++	USPAT
19	BRS	L19	0	(co-simulation) and FPGA and (state adj information) and emulation and HDL and Java	USPAT
20	BRS	L20	10	(co-simulation) and FPGA and (state adj information) and emulation and HDL	USPAT
21	BRS	L21	1	"5768567".pn. and switch	USPAT